Reduced Switches Based Three-Phase Multi-Level Inverter for Grid Integration

CONFERENCE PAPER · MARCH 2015

READS
51

5 AUTHORS, INCLUDING:

Ahmed Salem
4 PUBLICATIONS **2** CITATIONS
SEE PROFILE

Emad M. Ahmed
Aswan University
25 PUBLICATIONS **61** CITATIONS
SEE PROFILE

Reduced Switches Based Three-Phase Multi-Level Inverter for Grid Integration

Ahmed Salem[1], Emad M. Ahmed[1a], Mahrous Ahmed[1], Mohamed Orabi[1b], Afef Ben Abdelghani[2]
[1]APEARC, Faculty of Engineering, Aswan University, Aswan 81542, Egypt
[2] Electrical Systems laboratory, National School of Engineering, Tunis
[a] eelbakoury@apearc.aswu.edu.eg, [b] orabi@ieee.org

***Abstract*— this paper presents a novel three-phase Multi-Level Inverter (MLI). The proposed inverter operates with symmetrical DC power sources and low frequency modulation technique as well. The main contribution of the proposed topology is the total number of the active power switches used to generate the same number of levels compared to the previous topology is reduced by 25 %. Therefore, it is expected that the proposed inverter has high efficiency and low control complexity due to the decreased number of the power switches. The operation of the proposed inverter has been conducted by experimental results. Moreover, a comparison between the proposed inverter and the previous work is also included.**

Keywords—Three-phase multi-level inverter, low frequency modulation technique, symmetrical DC power sources.

I. INTRODUCTION

In recent decades, the demand for high voltage, high power inverters that capable to transfer a high power, has increased due to the industrial and residential demands. However, the traditional converters rating power are limited to the rated power of the used semiconductor devices and the allowed switching frequencies. The idea of introducing multilevel inverters strongly has appeared to overcome the previous traditional inverters drawbacks.

The general concept of multi-level inverter is to utilize isolated dc sources or a bank of series capacitors to produce ac waveforms with higher amplitude. The salient advantages of these inverters are small output voltage step, which results in high power quality, low harmonic components, better electromagnetic compatibility, and low switching losses [1]-[5].

There are three conventional types of power MLI topologies, named as neutral point clamped (NPC) [7], flying capacitors (FCs) [8] and cascaded H-Bridge (CHB) multi-level inverters [9]. Each of them have some advantages and some drawbacks regarding to the output voltage levels, the count of the used components, switching stresses and harmonic contents. However, the cascaded H-Bridge inverter requires the least number of components among all three conventional multi-level inverters topologies to achieve the same number of voltage levels [6].

New topologies have presented in the recent years focusing on minimizing the basic MLI topologies drawbacks. Such as multi-level DC link (MLDCL) [10], where a topology consist of basic cells connected in series is presented, each cell produce E DC voltage or 0 DC voltage. Across the connected cells, there is an H-bridge used to invert the polarity of the synthesized voltage, the required number of active switches is *m+3*, where *m* is the output voltage level number per phase.

In [11], the authors have introduced a topology named transistor-clamped H-bridge (TCHB) as a power cell that can produce a five-level per phase on the output voltage instead of three-level as with the conventional H-bridge. It requires per cell: two capacitors, four diodes and five switches; one of them is bidirectional switch.

In [12] and [13], the authors have produced the needed output voltage levels by series connected cells like in [10] in order to produce four levels in voltage per pole. Instead of using H-bridge to change the voltage polarities, it uses simply the phase shift relationship between the three legs voltages, by subtracts each leg's voltage with the neighboring one to produce the line voltage. Generally, more topologies have been attempt to reduce the total number of switches [10]-[13] and [14].

The aim of this paper is to reduce the components count compared with the conventional MLI topologies with keeping the same phase voltage levels. Doing this will reduced the converter size, losses, and the converter cost.

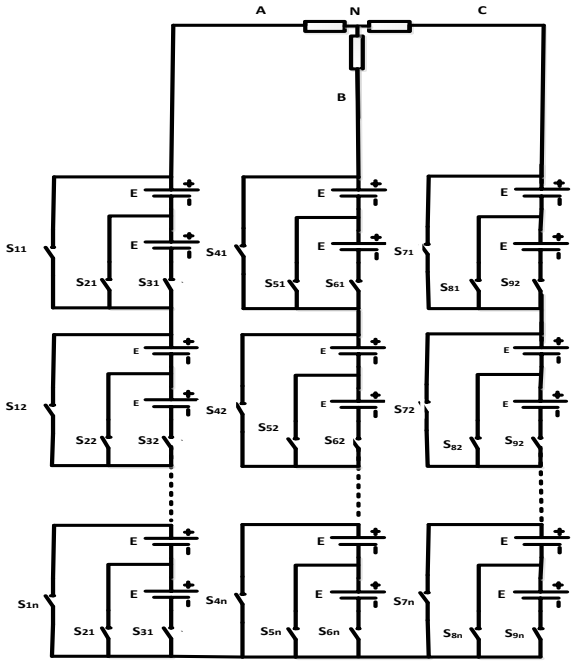
This paper is organized as follow: The structure of the proposed topology is introduced in section II. The proposed topology switching technique is demonstrated in section III. Investigating the operation of the proposed topology is presented in section IV. Comparing the proposed topology components with the previous topologies is developed in section V. Finally, a conclusion is introduced in section VI.

II. THE PROPOSED MLI TOPOLOGY

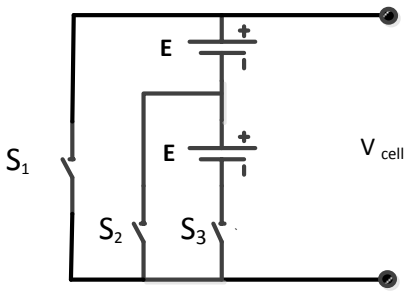
A new multi-level three-phase voltage source inverter with reduced components count is introduced in this paper. Figure 1 (a) shows the generalized power circuit of the proposed topology. It is formed through the arrangement of the primary basic cell in series configuration that is shown in Fig. 1 (b). Every basic cell consists of three switches S_1, S_2, S_3 and two symmetrical DC-power sources. This cell produces three voltage levels as explained in the following: when S_1 in ON state a 0 V_{dc} is produced on the cell terminal, when S_2 in ON state a E V_{dc} is produced on the cell output, when S_3 in ON state 2E V_{dc} is produced on the cell terminal ports. It should be noted that no switches could be operated in the ON at the same time in order to avoid a short circuit across the cell's DC power sources. Table

978-1-4799-7947-9/15$31.00©2015 IEEE

1 summarizes the different switching states and the corresponding output voltage of the proposed MLI topology.



(a) Proposed topology.



(b) Basic cell.

Fig. 1: The proposed MLI topology

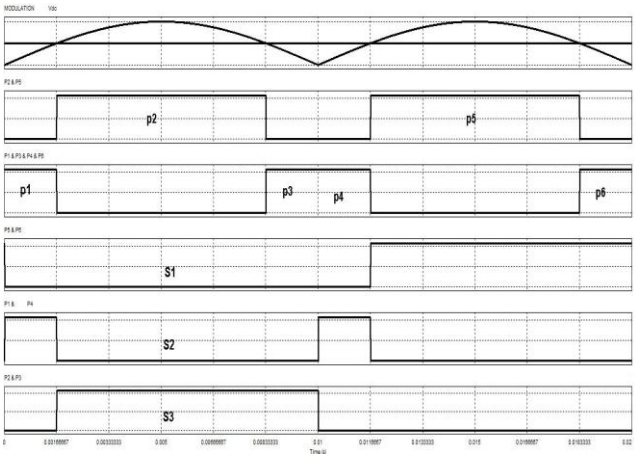


Fig. 2: The six pulses generation.

TABLE 1: SWITCHING STATES FOR THE BASIC CELL

Switching state	Switch			Basic-unit Output voltage
	S_1	S_2	S_3	
1	ON	OFF	OFF	0
2	OFF	ON	OFF	E
3	OFF	OFF	ON	2E

The proposed topology can be extended to have multi-levels more than three levels per cell, by forming a series configuration of the basic cell. The number of the generated output line voltage levels (M), output phase voltage levels (M_{ph}), the number of the used basic cells (N_{Cells}), the number of switches ($N_{Switches}$) and DC power supply ($N_{Sources}$) all are given in (1) - (5) respectively.

$$M = 4\,N_{Cells} + 1 \quad (1)$$

$$M_{ph} = 4\,N_{Cells} + 3 \quad (2)$$

$$N_{cells} = \frac{M-1}{4} \quad (3)$$

$$N_{Switches} = 3\,N_{Cells} \quad (4)$$

$$N_{Sources} = 2\,N_{Cells} \quad (5)$$

For example to obtain a nine voltage levels on the output line voltage (V_{ab}), according to the above equations, the investigated inverter produce five level per pole voltage (V_{ao}), eleven voltage levels per phase (V_{an}). Therefore, it is required for each arm to have two basic cells connected in series configuration, which is constructed from six switches and four symmetrical DC-power sources. The proposed multi-level inverter is recommended for the renewable energy resource especially the photovoltaic (PV) farms, at which there are enough DC energy sources to use.

In addition, the investigated topology is implemented as symmetrical MLI. However, it can be implemented as an asymmetry MLI, In this case, the voltage levels number increased dramatically as shown in Table. 2. The relationship between the used DC-power sources voltages values will be: double ratio (D-Ratio) (E, 2E volt) or triple ratio (TR-ratio) (E, 3E volt). In this case, the equations controlled the number of the generated levels are matching the one presented in [13].

III. PROPOSED INVERTER SWITCHING SCHEME

Driving the inverter switches according to low frequency modulation, a square wave pulses have been generated according to Table 3. There are twelve modes of operation per one cycle (50 Hz). The driver signals for arm **B** and arm **C** are shifted by 120°, -120°, respectively. In order to produce three phase blanched output voltages, the MLI's switching scheme that is shown in Fig. 2 has to be accomplished.

The switching devices for each arm, fired by signals that are generated by Appling some logical operations on the six periods (P_1 to P_6). The six periods produced from the intersection of rectified sine wave with amplitude equal to (X volt), and a constant DC value equal to ($X/2$ volt), as shown in Fig. 2. As the

sine wave amplitude voltage (*X*) value varies, the switching signal width for each switch will vary also. Therefore, as a result the THD and the output voltage root mean square (V_{rms}) will be varying. Equations (6) to (8) describe the logical operation applied on (P_1 to P_6) to produce the required switching devices signals (S_1, S_2, S_3) for phase (A) as;

$$S_1 = P_5 + P_6 \quad (6)$$

$$S_2 = P_1 + P_4 \quad (7)$$

$$S_3 = P_2 + P_3 \quad (8)$$

Where + stands for logic OR.

TABLE 2: THE NUMBER OF VOLTAGES LEVELS WHEN USING ASYMMETRY DC POWER SOURCES

dc sources voltage ratio	Line levels (V_{ab})	Phase levels(V_{an})	Pole levels (V_{ao})
D-Ratio	**13**	**15**	**7**
TR-ratio	**17**	**19**	**9**

IV. EXPERIMENTAL RESULTS

In order to validate the proposed three-phase multi-level inverter, a 3-level per pole / 7-level per phase is chosen here as shown in Fig. 3. The circuit is built in laboratory and tested. The MLI was implemented and prototyped using the metal–oxide–semiconductor field-effect transistor (MOSFET) as switching devices and 60 volt DC-power supplies. The converter prototype has been experimentally tested to confirm the proposed topology. Figure 4 shows the prototype setup used for the proposed inverter, which includes six DC-power supplies, switching devices, measurement tools, digital signal processor (DSP) as the switching controller, THD power analyzer and three-phase resistive load.

The switching scheme circuit is implemented by using the digital signal processor (DSP28335) controller. The three different signals for the switching cell are shown in Fig. 5. It is clear that they are matching with the designed equation (6)-(8).

Similar to topologies proposed in [12], [13], [14], the proposed inverter has the benefit from the zero part in the pole voltage waveform to produce the positive and negative output needed voltage waveforms. As a result, the number of switching devices would be reduced.

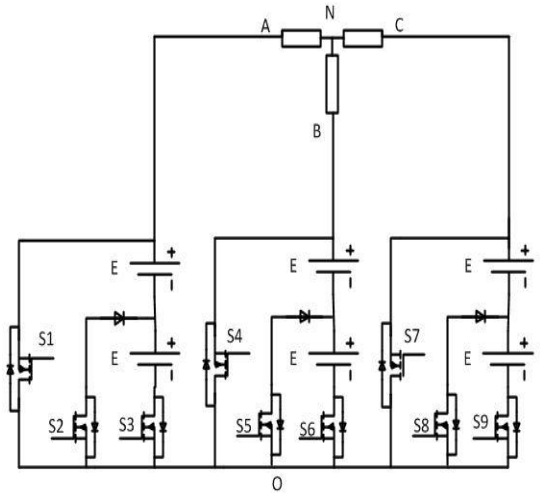


Fig. 3: Proposed 3-level per pole / 7-level per phase MLI topology.

TABLE 3: SWITCHING STATES FOR THE PRPOSED INVERTER

V_{ab}	V_{bc}	V_{ca}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
E	***-2E***	***E***	0	1	0	1	0	0	0	0	1
2E	***-2E***	***0***	0	0	1	1	0	0	0	0	1
2E	***-E***	***-E***	0	0	1	1	0	0	0	1	0
2E	***0***	***-2E***	0	0	1	1	0	0	1	0	0
E	***E***	***-2E***	0	0	1	0	1	0	1	0	0
0	***2E***	***-2E***	0	0	1	0	0	1	1	0	0
-E	***2E***	***-E***	0	1	0	0	0	1	1	0	0
-2E	***2E***	***0***	1	0	0	0	0	1	1	0	0
-2E	***E***	***E***	1	0	0	0	0	1	0	1	0
-2E	***0***	***2E***	1	0	0	0	0	1	0	0	1
-E	***-E***	***2E***	1	0	0	0	1	0	0	0	1
0	***-2E***	***2E***	1	0	0	1	0	0	0	0	1

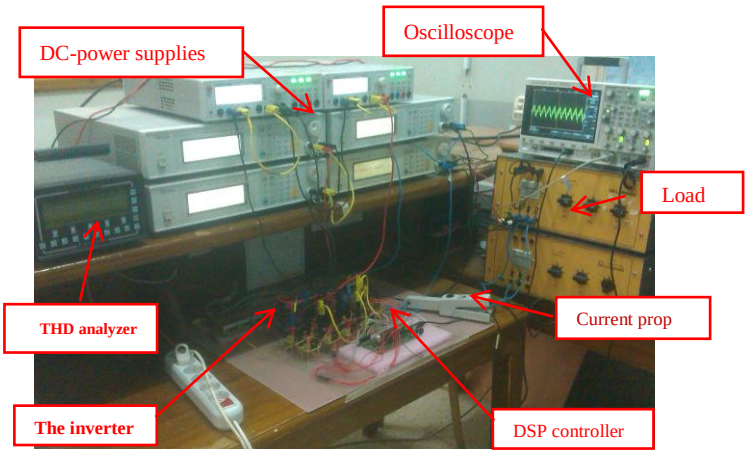


Fig. 4: Three-phase symmetrical multi-level converter prototype.

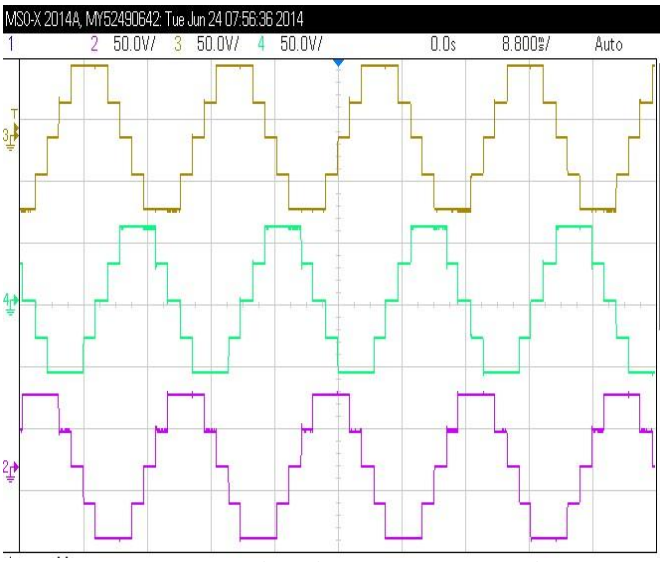


Fig. 7: The experimental waveforms for the line voltages waveforms (V_{ab}, V_{bc} and V_{ca}).

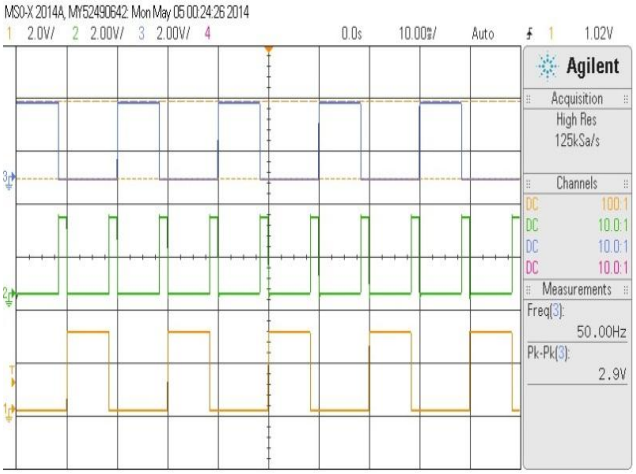


Fig.5: Switching scheme for S_1 ,S_2 and S_3.

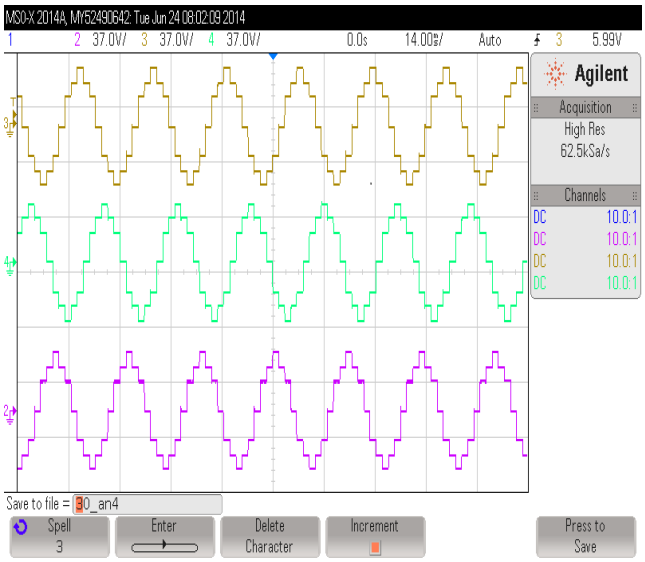


Fig. 8: The experimental results for the three phase voltages waveforms (V_{an}, V_{bn}, V_{cn}).

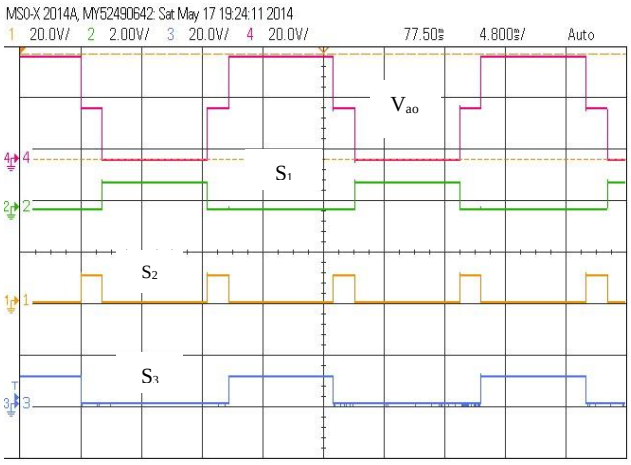


Fig. 6: Pole voltage (V_{ao}) and its switching signals for S_1, S_2 and S_3.

The experimental waveforms for the pole voltage (V_{ao}) and its switching pulses belong to phase **A** (S_1, S_2, S_3) are shown in Fig. 6. Also, the experimental outputs of the three-line voltages waveforms are shown in Fig. 7. The figure shows that each line voltage has five levels and has a phase shift of 120 degree between each other. Also, Fig. 8 shows the three phase voltages. As the pole voltages have three voltage levels (2E, E, 0 volt), the output line voltage have five voltages level (2E, E, 0,-2E,-E volt). The phase voltages are extracted from the line voltages; the five level line voltages produce seven levels on the output phase voltages, i.e. (E V_{dc}, $\frac{4}{3}$ E V_{dc}, $\frac{2}{3}$ E V_{dc}, 0 Vdc, - E V_{dc}, $\frac{-4}{3}$ E V_{dc}, $\frac{-2}{3}$ E V_{dc}).

A three phase resistive load of 40 Ω connected across the output terminals of the inverter, the experimental waveforms for line to line voltage, phase voltage and phase current all are shown in Fig. 9.

THD value is changed due to the modulation signal amplitude varying, therefore, Fig. 10 shows the THD for the line voltage against varying in sine wave signal amplitude. The figures illustrates that as the modulation amplitude (X) increases, the THD values decreases. As the modulation amplitude is chosen 1, the resultant THD of the line voltage is only 16.88%.

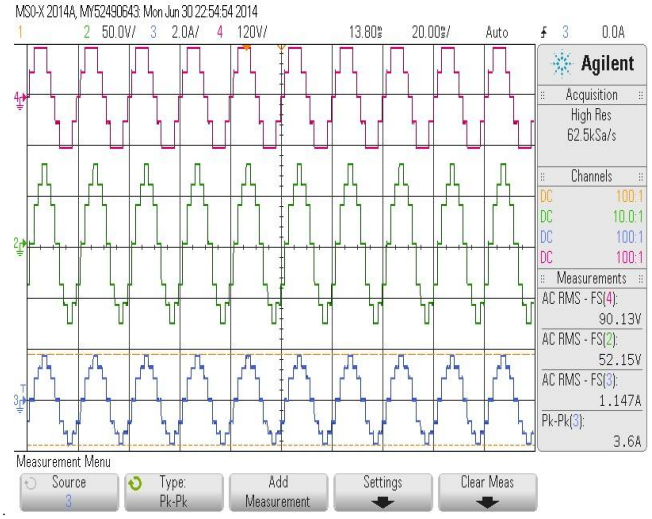


Fig. 9. The experimental output voltages waveforms: the line voltage, phase voltage and line current, respectively.

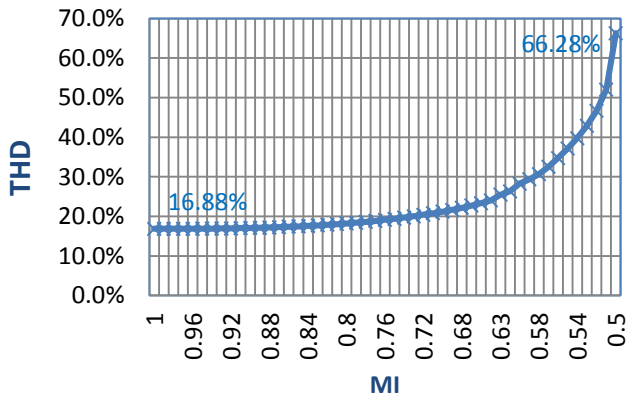


Fig. 10: The THD of the line voltage against varying in sin wave amplitude (*X*).

V. Comparison of the Proposed Topology with Previous Multi-Level Inverters

In order to ensure the feasibility of the proposed inverter, it is compared with the recent published topologies of multi-level inverter. They are introduced in [10], [12], [13], and [14]. The number of the voltage levels per pole is fixed for the comparison purpose. Also, the comparison is done based on symmetrical DC power supplies. For example, the presented topology in [13] is asymmetrical cascaded multi-level voltage source inverter and the proposed topology is symmetrical cascaded multi-level voltage source inverter, so the comparison is done for the topology in [13] by using symmetrical DC power sources only. Table. 4 summarizes this comparison and shows that the proposed topology has the smallest number of the active switches over other topologies.

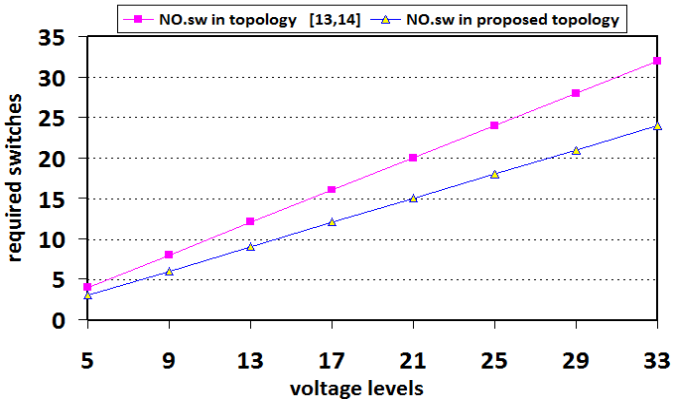
The topology in [13], [14] are the closest topologies to the proposed one, so a comparisons is carried out between them based on the required components and THD points of view. It is noticed that, the proposed topology in this paper requires reduced number of components to generate the same number of output pole voltage levels. It is about 25% reduction on the switches number as shown in Fig. 11 (a). In terms of the output voltage quality aspects as total harming distortion THD, the proposed inverter circuit seems to have better THD factor compared to the topologies presented in [13] and [14] as shown in Fig. 11(b).

VI. Conclusion

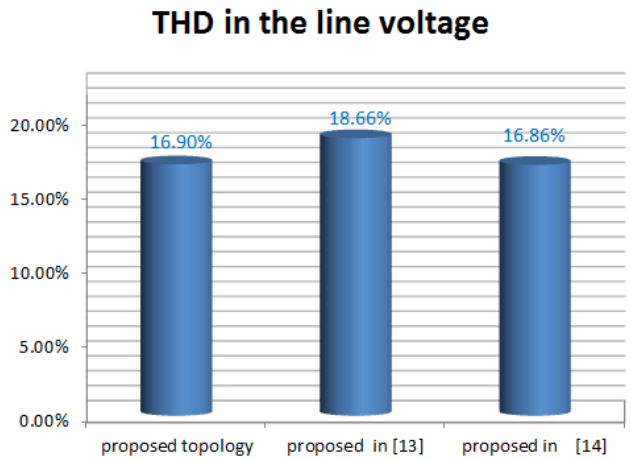
A novel three-phase multi-level inverter topology is proposed in this paper. The proposed inverter has the advantages of reducing the number of switches and gate drives circuits by 25 % compared with the conventional Multi-level inverter. Therefore, the proposed inverter exhibits the merits of simplified gate drive, high efficiency, low cost compared to the other topologies for the same number of phase voltages levels.

TABLE 4. Comparison between Proposed Topology and Other MLIs Topologies

Topology	FC	NPC	CHB	presented in [10]	presented in [12]	presented in [13]	presented in [14]	Proposed topology
No. of switches	**12**	**12**	**12**	**18**	**9**	**12**	**12**	**9**
Diodes	**12**	**18**	**12**	**18**	**21**	**12**	**12**	**15**
DC voltage sources	**1**	**1**	**3**	**3**	**1**	**6**	**6**	**6**
Capacitors	**9**	**2**	**0**	**0**	**2**	**0**	**0**	**0**



(a) The required switches number for the proposed topology and the proposed in [13], [14].



(b) THD for the proposed topology and the proposed in [13], [14].

Fig. 11: Comparison of the proposed topology features versus other topologies.

ACKNOWLEDGMENT

This work is funded in part by the Academy of Scientific Research & technology under Egypt-Tunis Collaboration project no. 39-13-A2 entitled by "Smart PV Micro-Grid System with Advanced Energy Management Control". Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the funding agencies.

REFERENCES

[1] Hammond, P.W, "A new approach to enhance power quality for medium voltage AC drives," IEEE Trans. Ind. Appl., 1997, 33, (1), pp. 202–208

[2] S. J. Park, F. S. Kang, M. H. Lee, and C. U. Kim, "A new single-phase five level PWM inverter employing a deadbeat control scheme," IEEE Trans.Power Electron., vol. 18, no. 18, pp. 831–843, May 2003.

[3] Agelidis, V. G., Baker, D. M., Lawrance, W. B., and Nayar, C. V.,"A multilevel PWM inverter topology for photovoltaic applications," Proceedings of the IEEE International symposium on Industrial Electronics, Vol. 2, pp. 589-594, July 1997, Portugal, Guimaraes.

[4] Gui-Jia Su, "Multilevel DC-Link Inverter", IEEE TRANS.IND. APPLICATIONS, vol. 41, no. 3, may/june 2005.

[5] M. Calais, L. J. Borle, and V. G. Agelidis, "Analysis of multicarrier PWM methods for a single-phase five-level inverter," in Proc. 32nd Annu. IEEE PESC, Jun. 17–21, 2001, vol. 3, pp. 1173–1178.

[6] Abdelaziz Fri, Rachid El Bachtiri, Abdelaziz El Ghzizal, "Basic topologies of a three-phase inverter (5l) for a photovoltaic system controlled by multi-carrier spwm," Journal of Theoretical and Applied Information Technology, 10th september 2013. vol. 55 no.1

[7] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Appl., vol. 1A-17, no. 5, pp. 518-523,

[8] M. F. Escalante, J. C. Vannier, and A. Arzande, "Flying capacitor multi-level inverters and DTC motor drive applications," IEEE Trans. Ind.Electron., vol. 49, no. 4, pp. 809–815, Aug. 2002.

[9] M. Malinowski, K. Gopakumar, J. Rodriguez, M. Pérez., "A Survey on Cascaded Multi-level Inverters," IEEE Trans Ind. Electron., vol. 57,no.7, pp. 2197-2206, 2010.

[10] S. Nagaraja Rao , D.V. Ashok Kumar, Ch. Sai Babu, "New Multi-levelInverter Topology with reduced number of Switches using Advanced ModulationStrategies," 2013 International Conference on Power, Energy and Control (ICPEC).

[11] Nasrudin Abd. Rahim, Mohamad Fathi Mohamad Elias, and Wooi Ping Hew, "Transistor-Clamped H-Bridge Based Cascaded Multi-level Inverter With New Method of Capacitor Voltage Balancing," IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 60, NO. 8, AUGUST 2013

[12] E.A. Mahrous, N.A. Rahim and W.P. Hew, "Three-phase three-level voltage source inverter with low switching frequency based on thetwo-level inverter topology," IET Electr. Power Appl., 2007, 1, (4), pp. 637 – 641

[13] Hamza Belkamel, Saad Mekhilef, Ammar Masaoud, Mohsen Abdel Naeim, "Novel three-phase asymmetrical cascaded multi-level voltage source inverter," IET Power Electron., 2013, Vol. 6, Iss. 8, pp. 1696–1706

[14] Ahmed Salem, Emad M. Ahmed, Mohamed Orabi, andAfef Ben Abdelghani, "Novel Three-Phase Multi-level Voltage Source Inverter with Reduced No. of Switches," The Fifth International Renewable Energy Congress, 14-WEN-386-O, 2014